REMARKS

Introductory Comments:

Claims 1-3, 5-15, and 17-26 are pending in the application. Claims 13-15 and 17-26 are allowed. Claims 1-3 and 6-12 are rejected under 35 U.S.C. §103(a) as being unpatentable over *Fuchs et al.* (6,141,770) in view of *Williams* (6,247,143). Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over *Fuchs et al.* in view of *Golshan* (6,671,841). The Applicant respectfully requests reconsideration of claims 1-3 and 5-12.

In Response To The Claim Rejections:

According to the Final Office Action, claim 1 is rejected because *Fuchs* discloses a fault tolerant processing circuit that comprises at least three processor groupings each of said at least three processor groupings having a plurality of processor grouping inputs and a plurality of processor grouping outputs (Figures 1 and 3), a processor system clock coupled to the fault tolerant processing circuit (Abstract), a synchronizing circuit comprising a plurality of output synchronizers (Abstract, column 7: lines 1-8, column 10: lines 8-11), a logic circuit in operative communication with said synchronizing circuit (Figures 3 and 6), said logic circuit comprising a fault detection circuit and a fault mask circuit (Figure 3, column 7: lines 24-43, column 9: lines 4-6, column 10: line 28 - column 11: line 14), said logic circuit adapted to compare said plurality of processor group outputs to detect errors in any one of said plurality of processor group outputs through selecting bits from the processor group outputs (Figure 3, column 10: line 28 - column 11: line 14), and a control logic circuit for resetting each of said at least three processor groups when none of said at least three processor groups is in a majority of said processor groups (Figure 6, Abstract, column 13: lines 1-42), wherein said fault mask circuit is adapted to mask the output of a respective processor grouping associated with a detected error and signal a detected error (column 9: lines 4-6). The Final Office Action recognizes that *Fuchs* does not clearly disclose wherein the bit selection is generated as a function of whether a first one of the plurality of processor group outputs is synchronous or asynchronous.

The Final Office Action alleges that *Williams* discloses a fault tolerant system that selects and compares the outputs of processor units, wherein the processor units can be synchronous or asynchronous with one another (Figure 3, Abstract, column 2: lines 49-67, column 3: line 64 -column 4: line 25).

In response to this rejection, the Applicant amends claim 1 to include that the processor groupings are "homogenous," and that "at least one of said plurality of processor group outputs

is asynchronous," in accordance with paragraph [0040] and Figure 2. No new matter has been added. Neither *Fuchs* nor *Williams* teach or suggest that the processor groupings are homogenous wherein one of the outputs of the processor groupings is asynchronous. Because the elements of claim 1 are not taught in the references either alone or in combination, claim 1 is believed to be new and non-obvious.

The *Fuchs* system is drawn to a fault tolerant computer system requiring that the processors operate in "strict 'lock-step.' " (Abstract.) More importantly, *Fuchs* does not teach or suggest that the processors may operate asynchronously. Rather, *Fuchs* teaches away from this combination by requiring synchronous (lock-step) operation.

The *Williams* system is directed towards I/O handling for a multiprocessor computer system requiring buffering of I/O operations or coordination with the processors originating the I/O operations. (Abstract.) More importantly, *Williams* does not disclose or suggest that the processors are homogenous. Instead, *Williams* teaches away from this element by including buffering of I/O operations or coordination with the processors originating the I/O operations.

Even if the references taught each and every element of the claims and did not teach away from the combination thereof, a combination of *Fuchs* and *Williams* would be clearly inferior to Applicant's claimed system. To start with, *Williams* operates at the I/O operations level and not the I/O signal level; this would cause greater system performance degradation than Applicant's system and would require hardware and software functionality and complexity to implement, were it combined with the *Fuchs* synchronous system.

Further, *Williams* requires that processor sets be able to issue progress signals and react to stall requests triggered by other processor sets and to manage by processor set external hardware in order to maintain synchronization. Therefore, *Williams* further necessitates a more difficult and costlier performance and operations analysis for use by computer system designers and system users; and in order to use COTS processors, it necessitates operating system software and application software modification/accommodation to implement.

For retaining I/O operation synchronization between the asynchronous processor sets, *Williams* requires progress indications with corresponding acknowledgements from the Monitor and allows interrupts only at progress indication synchronization points. (Column 5, lines 27-32.) This necessitates that application and operating system software accommodate this approach by modifying existing implementations and future software design techniques to correctly implement progress stalling (particularly when used with COTS processors). Because of time to market, cost, complexity, and risk issues, this is

vastly inferior to Applicant's claimed system. Additionally, as most modern computer systems demand high performance, real time computer applications with *Williams's* degree of handshaking between hardware and software will cause algorithm execution overhead, thereby precluding a *Williams* computer based solution as applied to *Fuchs*.

Claim 1 provides asynchronous system synchronization while restricting implementations to the use of homogeneous processors (CPUs) and by providing individual signal synchronization to remove signal skew across clock edges. This does not require additional feedback or protocol to be added to the processors (CPUs) hardware or software necessary to throttle algorithm execution. This eliminates the feedback from the buffer and voting logic incurred by *Williams*. This also eliminates progress signaling, with its comparatively large execution overhead and complexity costs, incurred by *Williams* processing sets. This further enables the use of COTS processors without modifications necessitated by *Williams'* technique. This also enables the use of traditional software solutions and the reusability of existing software made impossible by *Williams'* technique.

"Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1672, 1577, 221 USPQ 929, 933 (Fed.Cir. 1984). Even if all the elements of Applicant's invention are disclosed in various prior art references, the claimed invention taken as a whole cannot be said to be obvious without some reason given in the prior art why one of ordinary skill would have been prompted to combine the teachings of the references to arrive at the claimed invention.

In other words, "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Fritch, 972 F.2d 1260, 1266, 12 USPQ2d 1780, 1783-84 (Fed.Cir. 1992) citing In re Gordon, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed.Cir. 1984).

Applicant therefore submits that the combination of *Fuchs* and *Williams* would not render obvious Applicant's claimed system because *Fuchs* or *Williams*, either alone or in combination, do not disclose or suggest synchronous and asynchronous signal processing for homogenous processors whereby one of the outputs is asynchronous. Therefore, because no teaching or suggestion is found in either of the references for the limitations in claim 1, and because both references teach away from a combination thereof, Applicant respectfully requests the Examiner to reconsider this rejection.

Claims 2-3 and 5-12 depend from the amended claim 1 and are believed to be allowable for at least the aforementioned reasons.

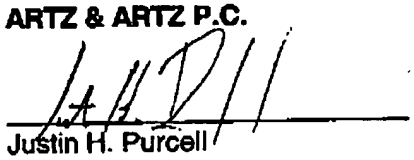
As mentioned, claim 5 is also rejected under 35 U.S.C. §103(a) as being unpatentable over *Fuchs* et al. in view of *Golshan*. As was discussed above, claim 5 depends from claim 1 and is believed to be allowable for at least the aforementioned reasons.

In view of the aforementioned remarks, it is respectfully submitted that all pending claims are in a condition for allowance. A notice of allowability is therefore respectfully solicited. Please charge any fees required in the filing of this amendment to Deposit Account 50-0476.

The Examiner is invited to contact the undersigned at (248) 223-9500 if any unresolved matters remain.

Respectfully Submitted,

ARTZ & ARTZ P.C.



Justin H. Purcell
Reg. No. 53,493
Artz & Artz, PC
28333 Telegraph Road, Suite 250
Southfield, MI 48034
(248) 223-9500

Dated: March 28, 2005